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claim.

Claims 1-3, 5, and 7-8 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 4,804,636 to Groover III et al. Claims 1-3 and 5-8 were rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 5,911,114 to Naem. Claim 4 was rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Naem. Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claim 1 is patentably distinct from the cited art for at least the following reasons.

Independent claim 1 relates to a semiconductor device comprising a Si substrate and a resistance element formed on the substrate. The resistance element comprises a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level. The second resistance pattern is electrically connected in series to the first resistance pattern to form the resistance element, and the second resistance pattern has an edge defined by the first resistance pattern.

Groover, as understood by Applicant, relates to a process for making VLSI integrated circuits and a local interconnect system, wherein first poly, second poly, and moat are all interconnected by a TiN local interconnect.

Applicant respectfully reiterates the request for clarification which was expressed in Applicant's January 2, 2003 response. More specifically, it is unclear what are the structures of Groover referred to in the Office Action which correspond to the elements of the claimed invention.

The Office Action states that Groover shows "a first resistance pattern (poly-Si) on the substrate at a first level and a second resistance pattern (source/drain or moat) provided adjacent the first resistance pattern at a second level (in the substrate) lower than the first

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level" (see Office Action, p. 2, ln. 21 through p. 3, ln. 1). The Office Action also states, in reference to Groover, that "[t]he second resistance pattern is formed in the substrate in the form of a silicide region (TiSi<sub>2</sub>)" (see id., p. 3, lns. 9-10).

As understood by Applicant, the TiSi<sub>2</sub> region and the source/drain region of Groover are distinct elements and are not coextensive (see Groover, Figs. 9a-9e).

The Office Action first states that the "source/drain or moat" of Groover corresponds to a second resistance pattern (see Office Action, p. 2, ln. 24), and later states that this alleged second resistance pattern has an edge defined by the first resistance pattern because the "moat is doped by a self aligning process" (see id., p. 3, lns. 3-4). The Office Action then states that the second resistance pattern is in the form of a "salicide region (TiSi<sub>2</sub>)" (see id., lns. 9-11).

It is respectfully submitted that, as depicted in Figs. 9a-9e of Groover, the "moat" and the "salicide region (TiSi<sub>2</sub>)" are distinct elements, and that the comments of the Office Action are accordingly unclear.

In any event, in the process of Groover, as understood by Applicant, sidewall oxide filaments are located adjacent to a polysilicon gate. The sidewall oxide filaments separate the polysilicon gate from the silicide regions on the source/drain regions (see Groover, col. 7, lns. 3-13; Figs. 1-2). The filaments must be located at the edge of the polysilicon gate in order to electrically isolate the gate from the source/drain regions. The titanium nitrate layer and the titanium silicide regions are apparently formed by depositing titanium metal "everywhere" and heating the substrate (see id., col. 7, lns. 22-30). The placement of the material deposited and of the titanium silicide regions formed by the depositing process are therefore apparently dependent upon the exterior boundaries of the sidewall oxide filaments, without any definition of an edge of either the upper or lower pattern by the

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other (see id., Figs. 1-2).

In contrast, as recited in independent claim 1, the second resistance pattern has an edge defined by the first resistance pattern. This formation of the second resistance pattern guarantees a high level of accuracy of the resistance.

Applicant finds no teaching or suggestion in Groover of a substrate and a resistance element formed on the substrate, the resistance element comprising a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being electrically connected in series to the first resistance pattern to form the resistance element, and the second resistance pattern having an edge defined by the first resistance pattern, as recited in independent claim 1.

In the section entitled "Response to Arguments," the Office Action states that "any material in known in the art of semiconductors provides resistance and this is a resistance pattern" (see Office Action, p. 6, Ins. 2-4). Applicant respectfully disagrees.

It is respectfully submitted that the specification and drawings of the present application clearly identify each element of the claimed invention. For example, the present application states in connection with the background for the claimed invention at p. 2, Ins. 11-16 that "[i]n semiconductor devices, resistance elements are formed generally by a patterning process of a polysilicon layer, wherein such a polysilicon layer may be formed on a diffusion region on a semiconductor substrate or on an insulation film covering the semiconductor."

Furthermore, Fig. 1 of the present application shows an example of a conventional polysilicon resistance element (see also p. 4, Ins. 5-6). In describing the resistance element of Fig. 1, the specification states that "[r]eferring to Fig. 1, there is provided a number of

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polysilicon resistance patterns 2 on a surface of a substrate (not shown) in a parallel relationship with each other, wherein the resistance patterns 2 are connected in series by conductor patterns 4 also provided on the substrate to form a desired resistance element having a desired resistance value" (see id., lns. 7-13; Fig. 1).

Fig. 3 of the present application corresponds to one embodiment of the present application. Referring to Fig. 3, the specification states that "... the polycide patterns 19 and the adjacent salicide regions 20B are connected at the contact holes 22 and 24 formed at respective ends thereof by the local interconnection patterns 26, to form a resistance element in which the polycide patterns 19 and the salicide regions 20B are connected in series" (see id., p. 13, lns. 3-10; Fig. 3). The specification also states that "... the polycide patterns 19, each having a width W and a length L, are arranged in a parallel relationship with each other with a mutual separation S. Thereby, it can be seen that the salicide regions 20B are between adjacent polycide patterns 19 with a width S and the same length L" (see id., lns. 11-22; Fig. 3).

It is therefore submitted that the elements of the recited claims of the present invention have been clearly described in the specification, and the statement in the Office Action that the resistance pattern of independent claim 1 corresponds to "any material in known in the art of semiconductors" (see Office Action, p. 6, lns. 2-4) is overly broad particularly in light of the clear description in the present application. The descriptive passages reproduced above are presented exemplarily for illustration within the present discussion, and are not seen nor intended to limit the present application to the specific examples identified above.

Furthermore, it is respectfully submitted that the Office Action improperly integrates distinct and independent elements of the prior art into a single structure, without

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teaching or suggestion in the cited art of such a singular structure. Namely, the Office Action contends that the sidewall oxide and gate dielectric together form a single upper resistance pattern (see Office Action, p. 6, lns. 4-8).

As understood by Applicant, however, Groover states that the sidewall oxide filaments separate the polysilicon gate from the silicide regions on the source/drain regions (see Groover, col. 7, lns. 11-13). It is respectfully submitted that there is no suggestion or motivation in Groover to combine these independent elements into a single resistance pattern, or that such a combination functions or may function as a single resistance pattern.

The Office Action states that Groover discloses a second resistance pattern having an edge defined by a first resistance pattern (see Office Action, p. 6, lns. 9-16). The Office Action also states that "... an LDD implant to form part of the second resistance pattern below the first resistance pattern comes after the gate polysilicon has by [sic] deposited and etched" (see id.). The Office Action further states: "[t]hus, the edge of the second resistance pattern is defined by the first resistance pattern" (see id.).

It is respectfully submitted that Groover does not disclose the definition of an edge of a second resistance pattern by a first resistance pattern.

As understood by Applicant, the section of Groover cited in support of this contention relates to a process flow for producing an integrated circuit. Beginning at step 6, the process includes the steps of growing a new gate oxide, depositing second polysilicon, patterning and etching poly 2 (see Groover, col. 21, lns. 5-45). The process continues with step 9, which according to Groover stated in its entirety: "[p]erform LDD implant if desired" (see id.). Groover is not seen to disclose or suggest that the LDD implant of step 9, purportedly (according to the Office Action) an equivalent to the second resistance pattern, has an edge in any way defined by the first resistance pattern, as recited

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in independent claim 1.

Accordingly, for at least the above reasons, Applicant submits that independent claim 1 is patentably distinct from Groover.

Naem, as understood by Applicant, relates to a method of simultaneously forming refractory metal salicide and local interconnects in an integrated circuit structure. Titanium and TiN films are deposited after formation of N+ and P+ junctions. The structure is annealed in a nitrogen ambient to form a salicide film on the exposed source, drain, and gate regions.

The Office Action states that Naem discloses "a first resistance pattern (on field oxide region)" and "a second resistance pattern (source/drain) provided adjacent the first resistance pattern" (see Office Action, p. 3, lns. 16-18).

As understood by Applicant, this reference to a first resistance pattern on the field oxide region corresponds to the polysilicon resistor (see Naem, col. 2, lns. 55-56) depicted in Figs. 1A-1E of Naem. It is respectfully submitted that the source/drain region depicted in Figs. 1A-1E of Naem does not have an edge defined by any part of the polysilicon resistor (see id., Figs. 1A-1E).

In contrast, as recited in independent claim 1 of the present application, the second resistance pattern has an edge defined by the first resistance pattern.

Applicant finds no teaching or suggestion in Naem of a substrate and a resistance element formed on the substrate, the resistance element comprising a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being electrically connected in series to the first resistance pattern to form the resistance element, and the second resistance pattern having an edge defined by the first

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resistance pattern, as recited in independent claim 1.

Accordingly, Applicant respectfully submits that independent claim 1 is patentably distinct from Naem.

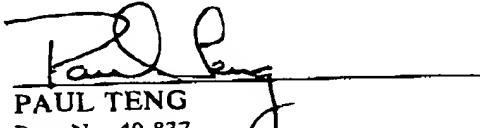
The Office is hereby authorized to charge any fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an additional extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Entry of this response and allowance of this application are respectfully requested.

Respectfully submitted,

  
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